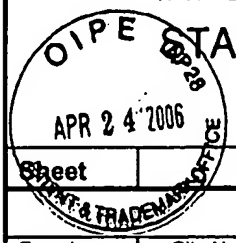
Substitute for Form 1449/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)



Complete if Known	
Application Number	10/665,970
Filing Date	September 18, 2003
First Named Inventor:	Soma et al.
Art Unit	2863
Examiner Name	Bryan Bui
Attorney Docket Number	4735.P005

Sheet	1	of	2

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Document Number Number-Kind Code[2] (if known)		Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
BB	1	US-	6,295,315 B1	09-25-2001	Frisch et al.	
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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No.[1]	Foreign Patent Document Country Code[3] Number[4] Kind Code[5] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T[6]

Examiner Signature		Date Considered	5/3/06

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				Examiner Name	Bryan Bui
Sheet	2	**of**	2	Attorney Docket Number	4735.P005

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No[1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	T[2]
BB	2	BOUWMAN, F. et al., "Application of Joint Time-Frequency Analysis in Mixed Signal Testing," Proc. IEEE International Test Conference, pp. 747-756, Washington, DC, 1994.	
	3	YAMAGUCHI, T.J. et al., "Dynamic Testing of ADCs Using Wavelet Transforms," Proc. IEEE International Test Conference, pp. 379-388, Washington, DC, 1997.	
	4	SUNTER, S. et al., "BIST for Phase-Locked Loops in Digital Applications," Proc. IEEE International Test Conference, pp. 532-540, Sept. 28-30, 1999, Atlantic City, NJ.	
	5	MASON, R. et al., "Mixed Signal DFT at GHz Frequencies," J. of Electronic Testing: Theory and Applications 15, pp. 31-39, 1999.	
	6	ROH, J. et al., "Subband Filtering Scheme for Analog and Mixed-Signal Circuit Testing," Proc. IEEE International Test Conference, pp. 221-229, Atlantic City, NJ, 1999.	
	7	YAMAGUCHI, T.J. et al., "Jitter Measurements of a PowerPC Microprocessor Using An Analytic Signal Method," Proc. IEEE International Test Conference, pp. 955-964, Atlantic City, NJ, 2000.	
	8	CHAN, A.H. et al., "A Synthesizable, Fast and High-Resolution Timing Measurement Device Using a Component-Invariant Vernier Delay Line," Proc. IEEE International Test Conference, pp. 858-867, Baltimore, MD, 2001.	
BB	9	BHUNIA, S. et al., "Dynamic Supply Current Testing of Analog Circuits Using Wavelet Transform," Proc. IEEE VLSI Test Symposium, pp. 302-307, Monterey, CA, 2002.	

Examiner Signature	BB	Date Considered	5/30/06

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